



Nano Manufacturing Challenges

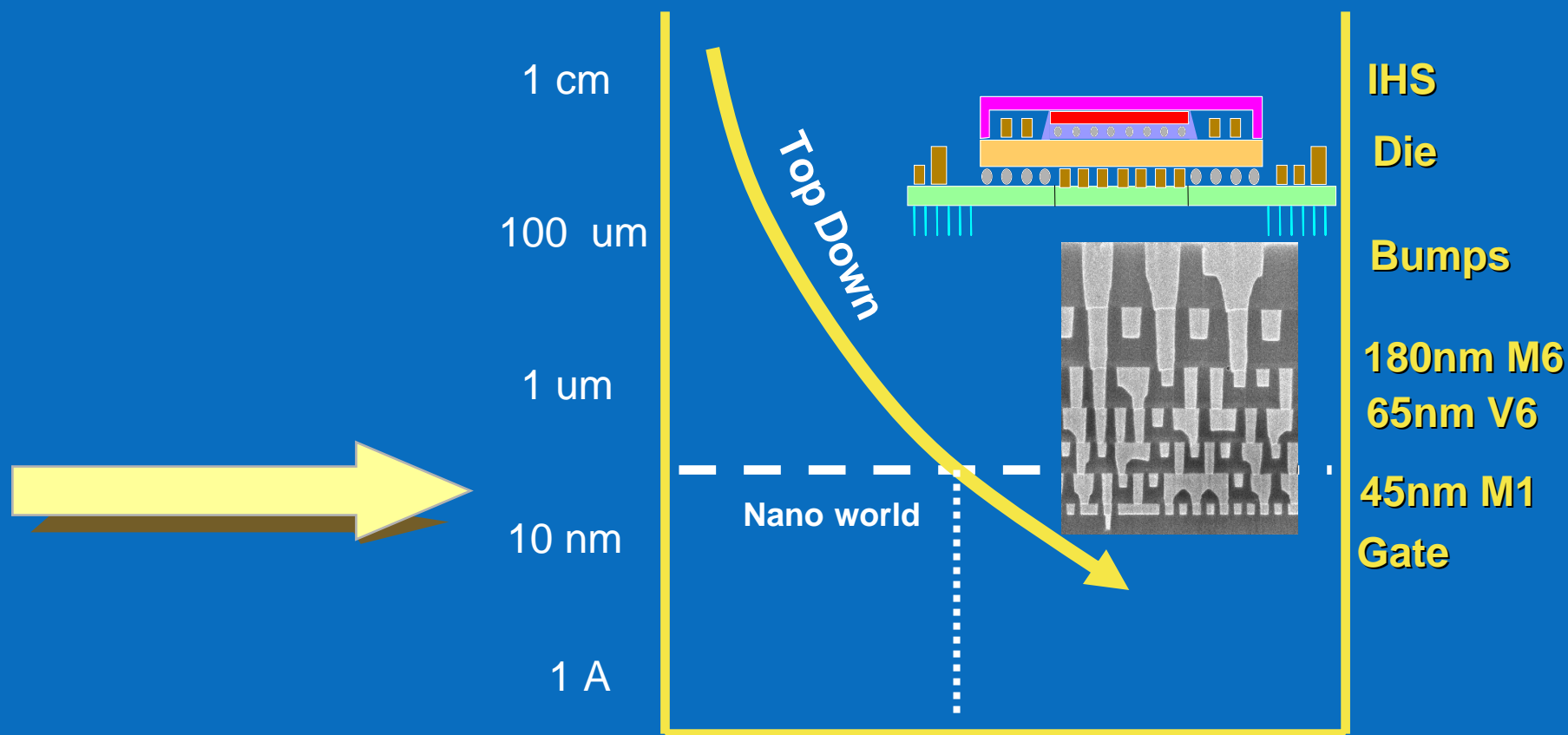
Mike Mayberry

VP, Director of Components Research
Technology and Manufacturing Group

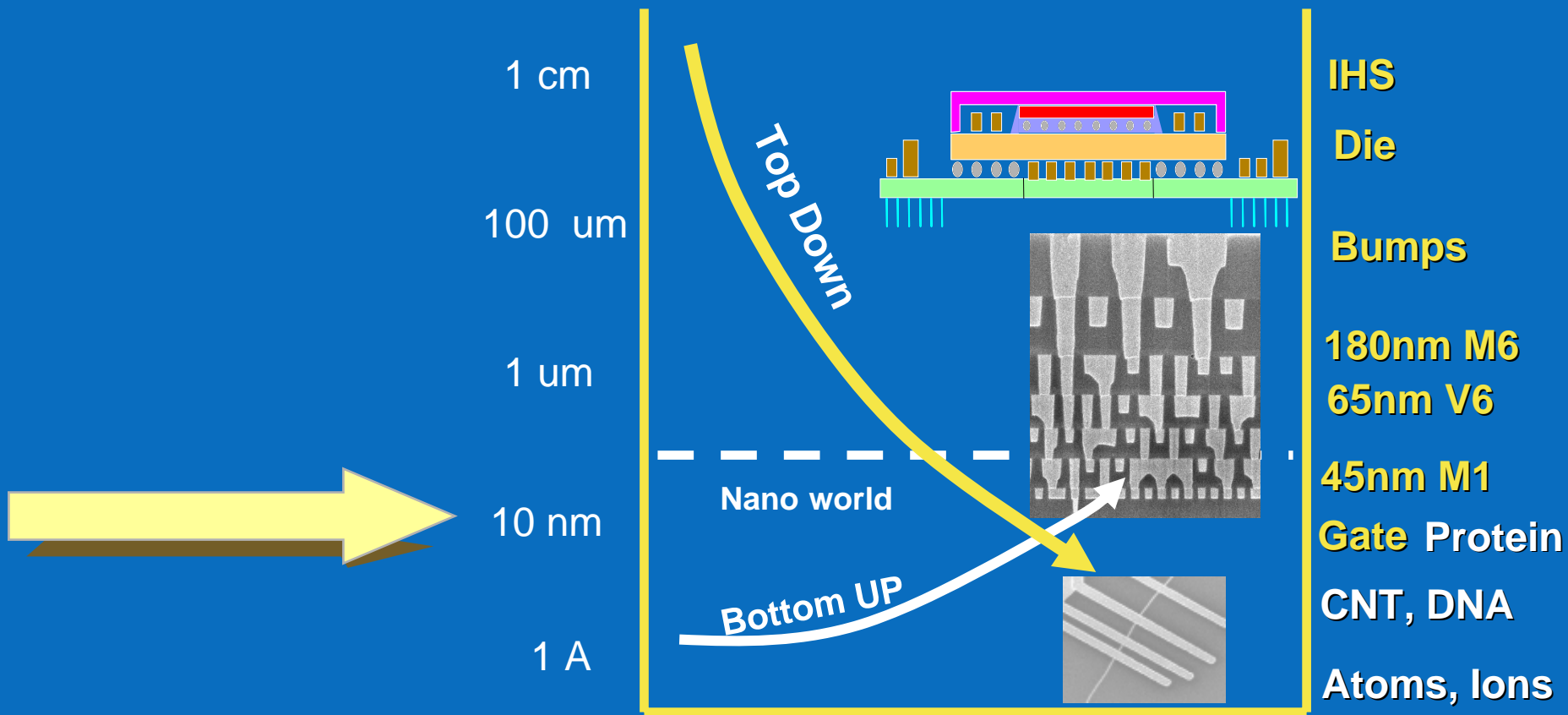
Not all Nano is created equal ...

... while commonly defined as lengths below 100nm, how you get there matters

Old News: Electronics has already entered the Nano Realm

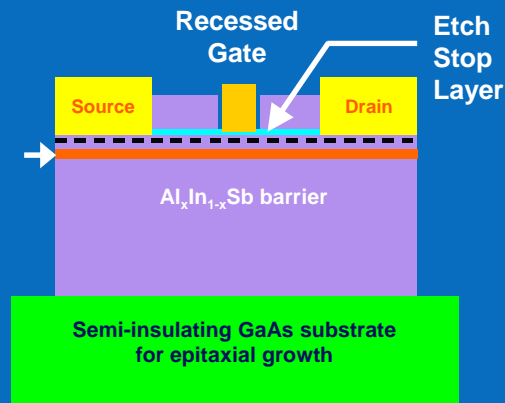
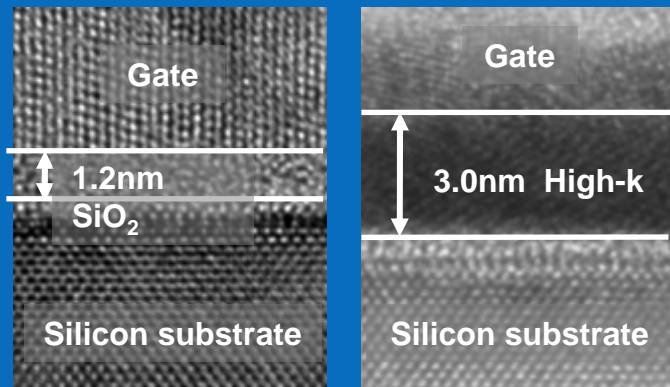


New News: Convergence between Top-Down Scaling and Bottoms-Up Construction



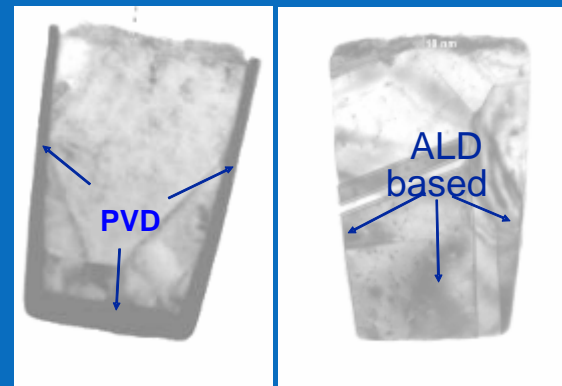
1D Nano and 2D Macro

Source: Intel



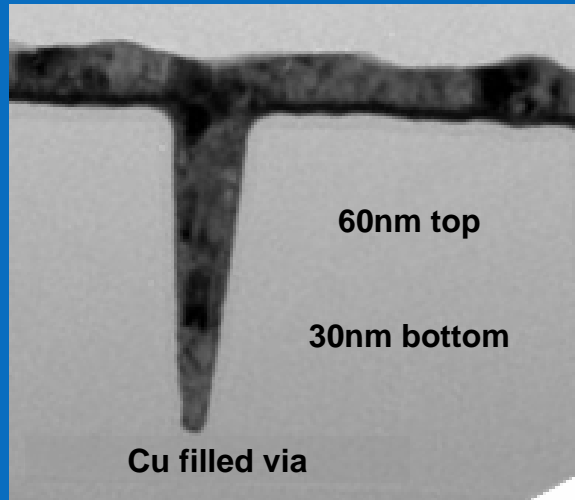
- Novel properties due to dimension, drives new materials
- Formed in place, attached to much larger structure
- Widely used in semi manufacturing

No Buzz



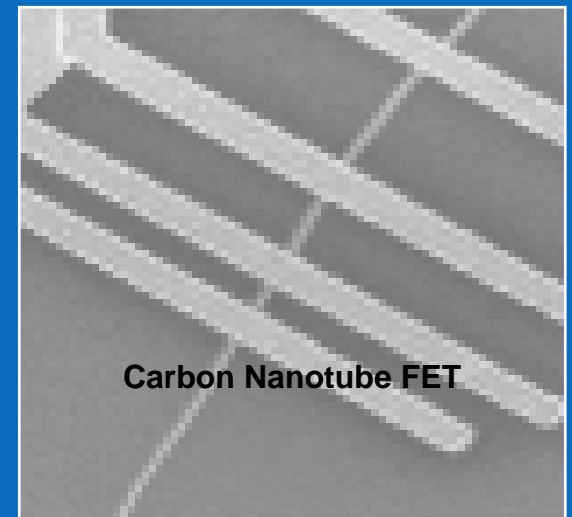
Source: Intel

2D Nano and 1D Macro



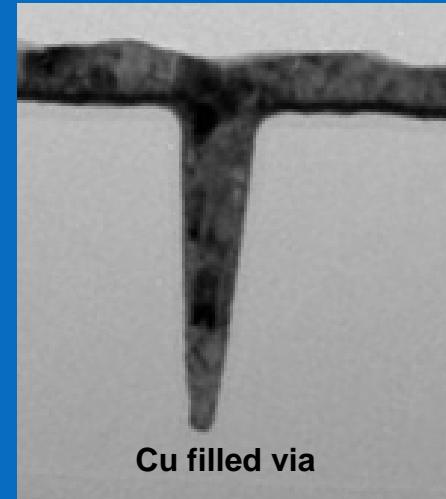
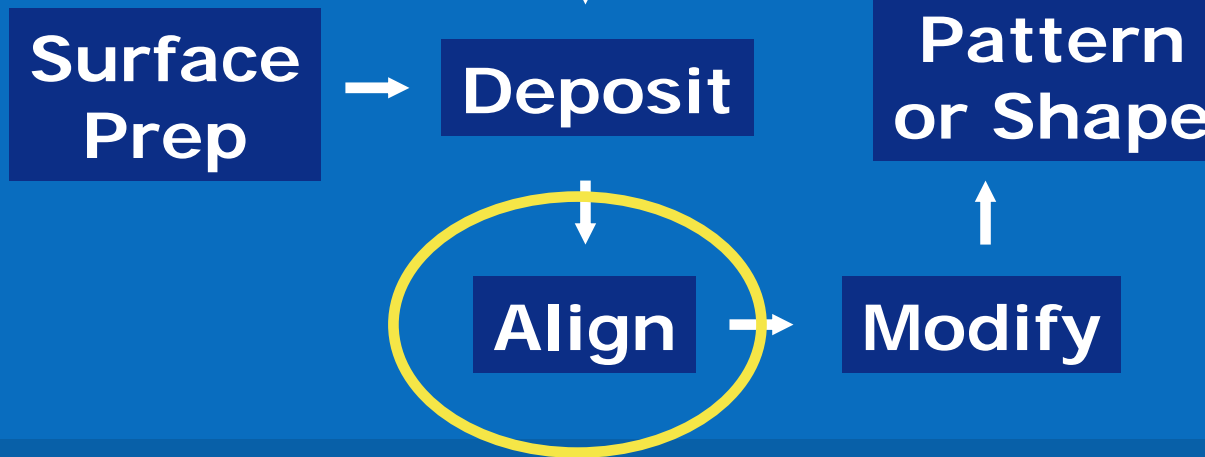
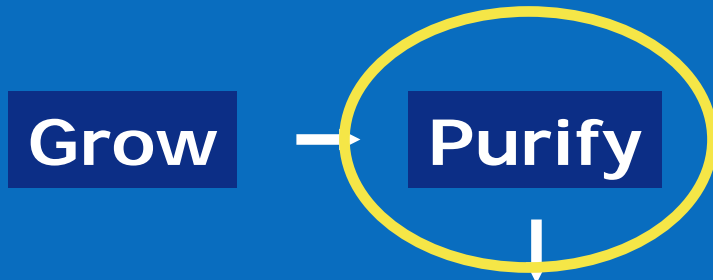
Source: Intel

- Novel properties due to dimension, drives new materials
- Formed in place, attached to much larger structure **No Buzz**
- ... or formed separately and integrated **Buzz**



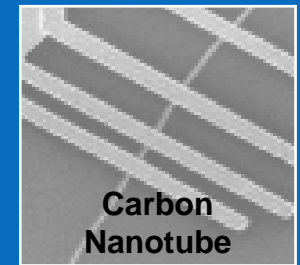
Source: Intel

Flow comparison



Cu filled via

Source: Intel



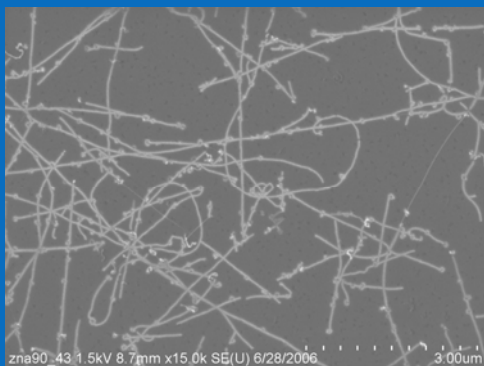
Carbon Nanotube

Source: Intel

It can be done ... on lab scale

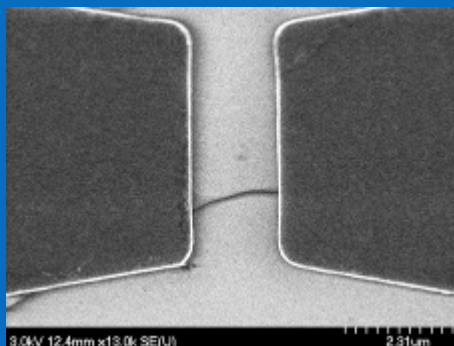
- Single wall CNT grown on catalyst
- Nanotube suspension
- Coupon application
- Dielectrophoresis to align
- Metallization for electrical contact
- High freq verification (20-50GHz, 2-5um)

Grow
Purify
Deposit
Align
Integrate
Verify



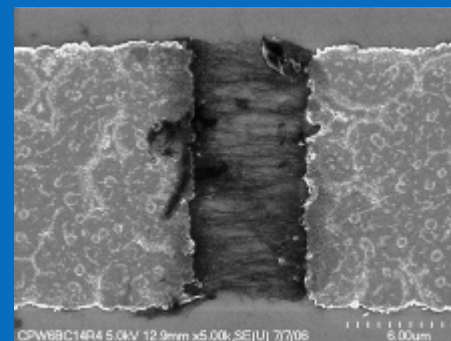
CNT as grown

Source: Intel



Aligned single CNT

Source: Intel



**Aligned CNT bundle
(few thousand CNT)**

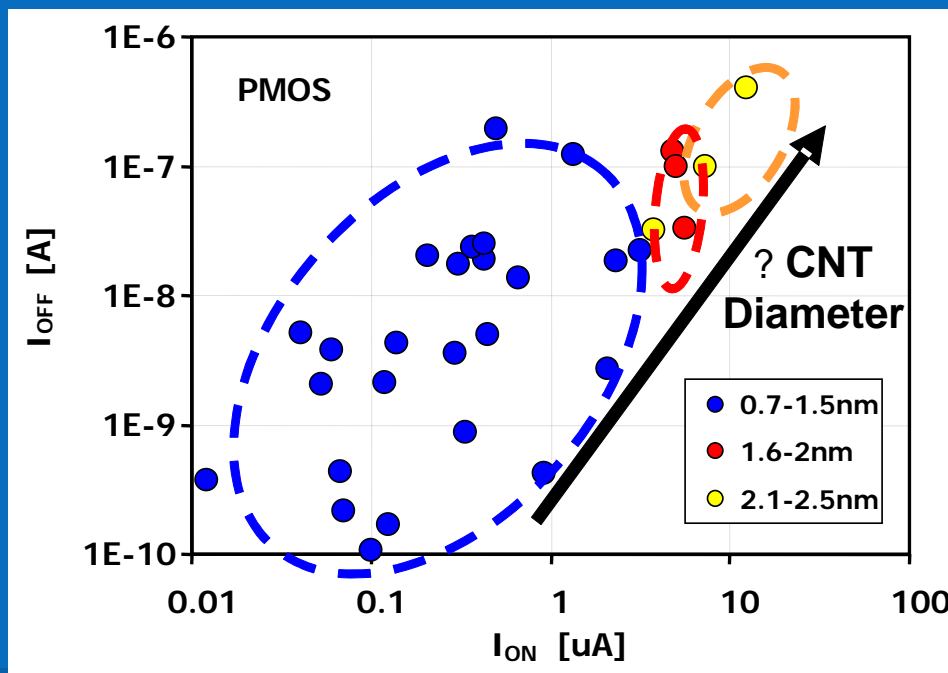
Source: Intel



Scaling up for Nanoelectronics

- Purification
 - Begin with clean starting materials
 - Control grow process to reduce variability
 - Remove undesirable contaminants

Possible



Source: Intel

Scaling up for Nanoelectronics

- Purification

- Begin with clean starting materials
- Control grow process to reduce variability
- Remove undesirable contaminants

Possible

- Alignment

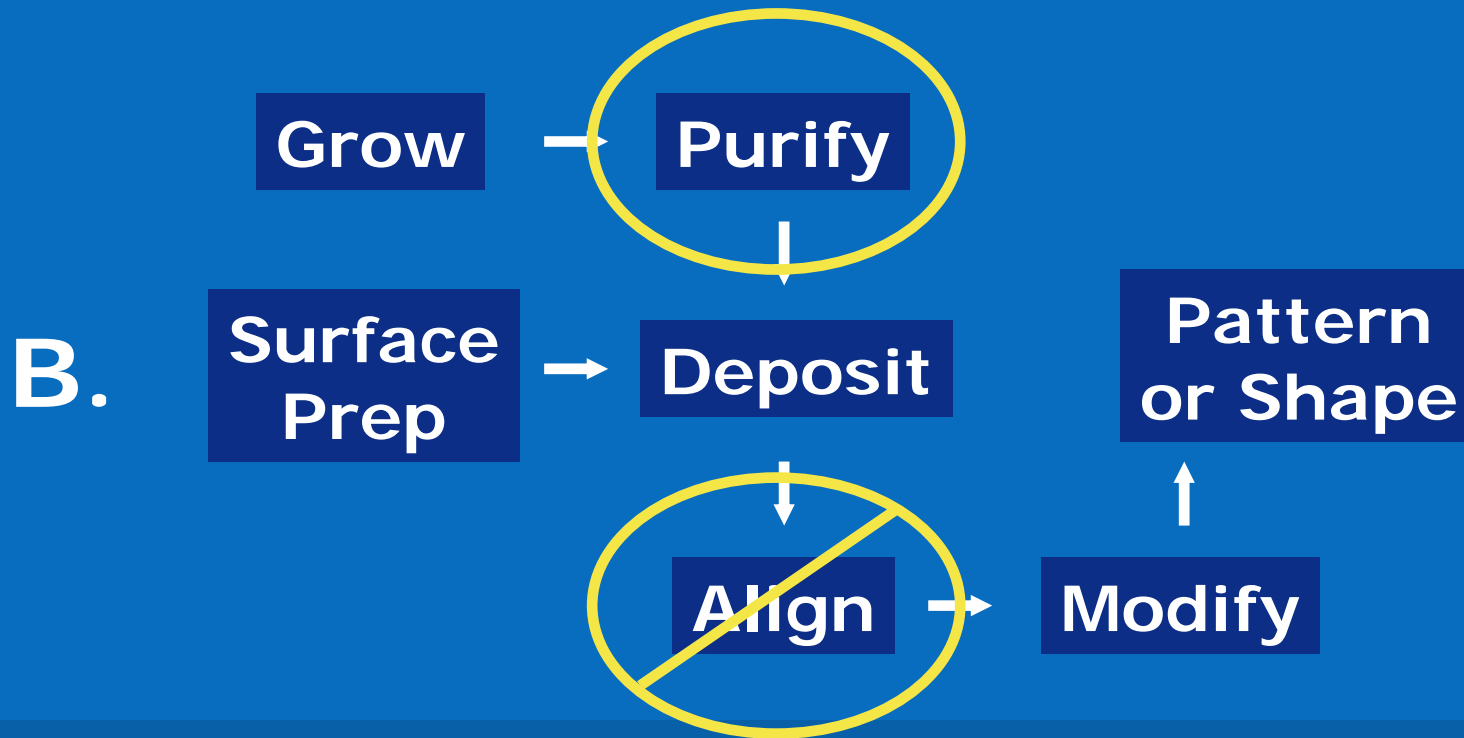
- In 2015 a leading edge logic device might have >50B transistors
- A critical layer might have 4 terabytes of pixels
- Placement requirements of a few nm with error rates $\ll 10^{-14}$

Difficult to imagine a solution

**What do you call a free
floating
3D nanomaterial?**

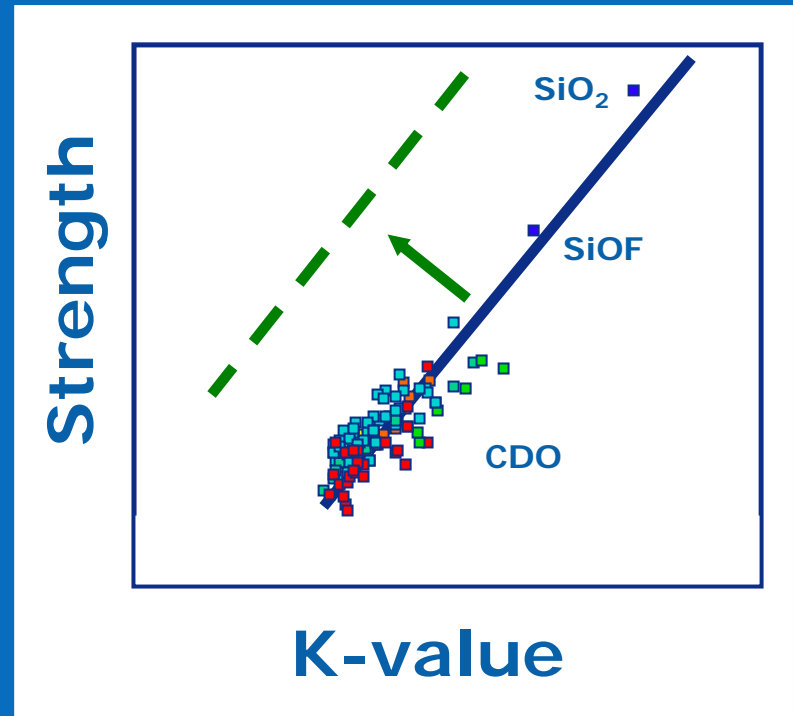
Answer: A particle

Opportunities for 3D Nano



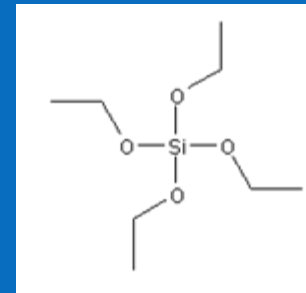
Defining Better Interconnect Dielectrics

- SiO_2 based dielectrics tend to follow same performance curve
 - Holds for a wide variety of precursor chemistries
 - How weak you tolerate determines how low you can go for k effective
- Migration from SiO_2 to SiOF to CDO were all difficult but also only incremental k improvement
- Opportunity if there is a way to move off the curve

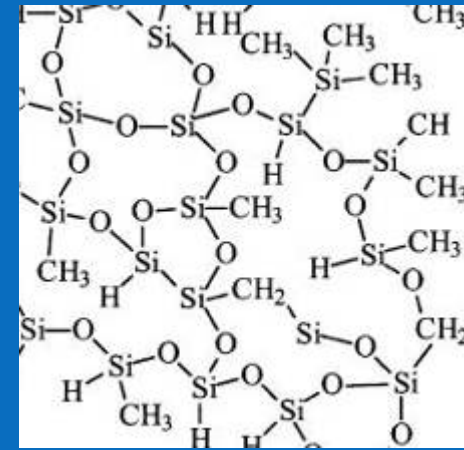


Porosity Options

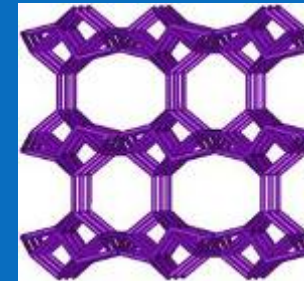
- Example porous ILD
 - About 25% porous (random)
 - Pore size ~2nm
 - At this level, pores are interconnected = extra integration challenges
- Ordered materials
 - Potentially higher porosity but lower interconnection, superior strength
 - Typically only available as spin-on coatings
- Polymers offer the potential of lower porosity and lower strength at equivalent k value



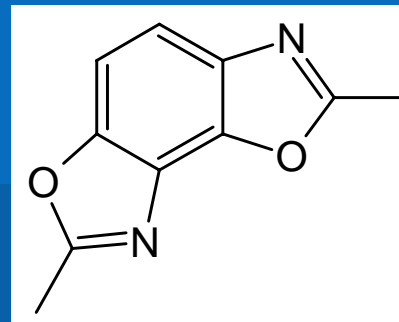
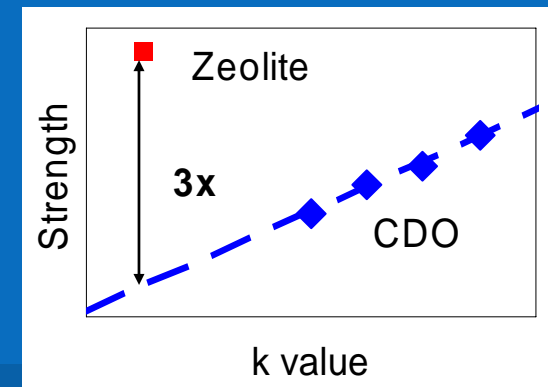
PECVD



Spin-on

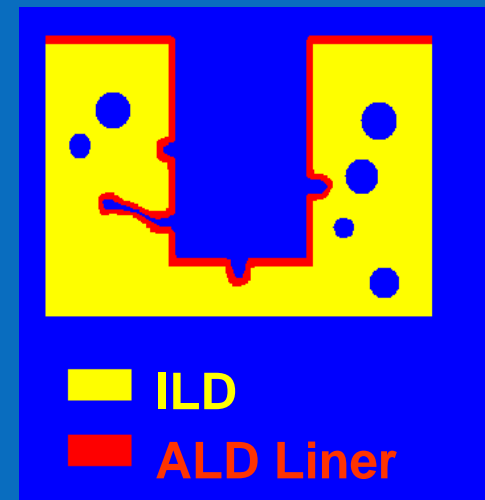
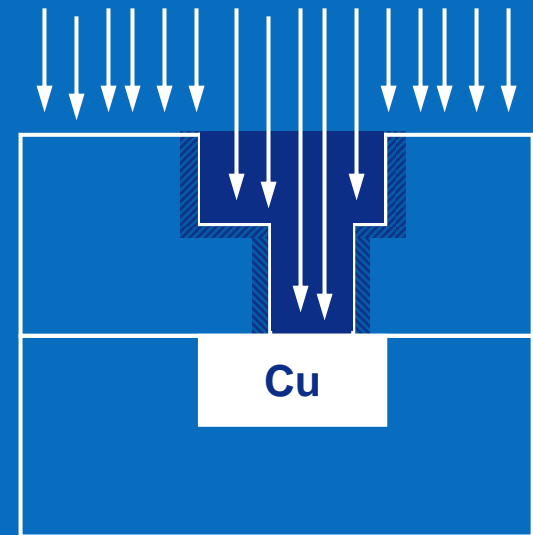


Source: Li et al, UCR, J Phys Chem, 2005



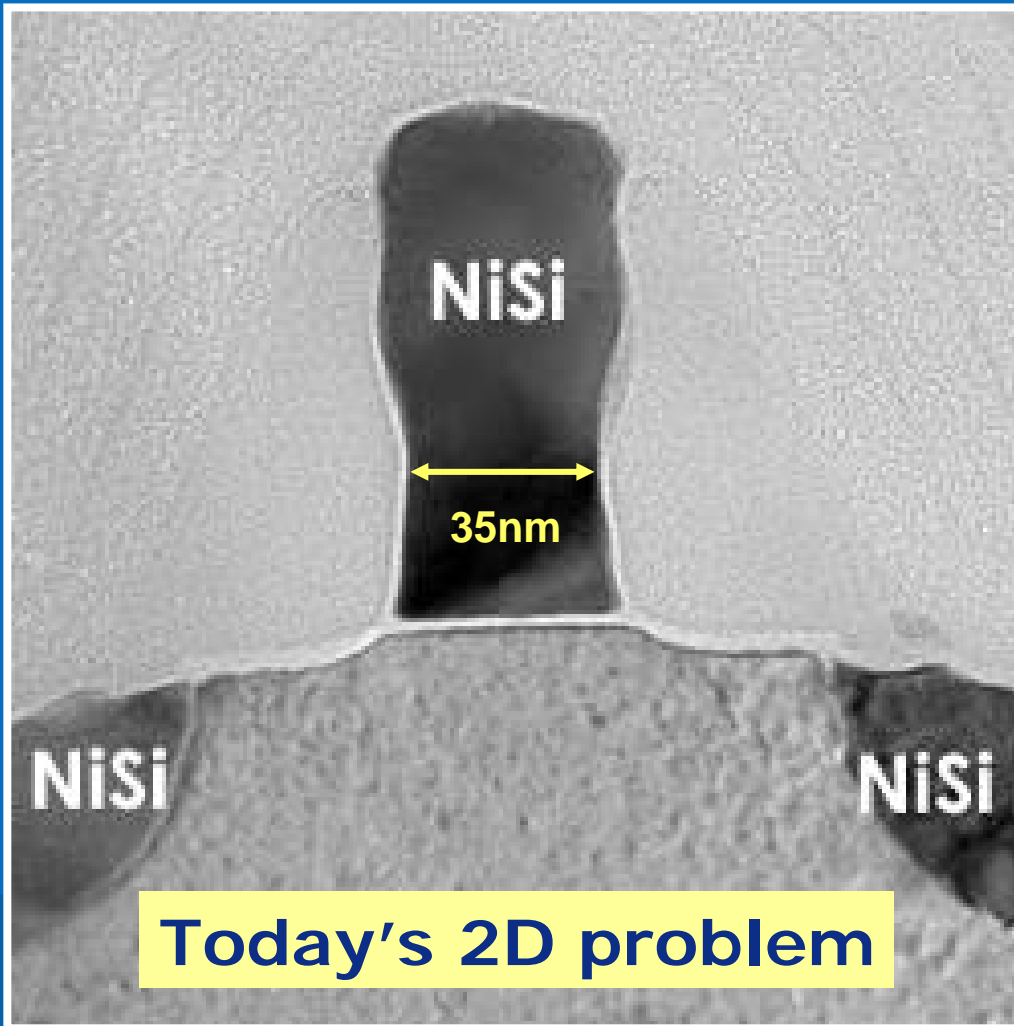
Integration

- Even if pores are unconnected as formed, subsequent patterning exposes a different surface
- Need to
 - Prevent damage to structure, particularly that affecting k_{EFF}
 - Smooth (seal) the surface for later conformal deposition
 - Good adhesion as deposited and over subsequent processing and also over a range of process conditions
- Could be accomplished with right combination of materials and surfaces

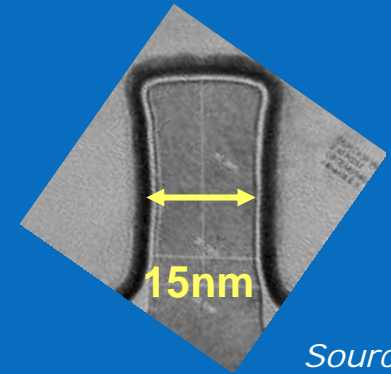


Lithography at Nanoscale

193nm light



13.5nm light



Source: Intel

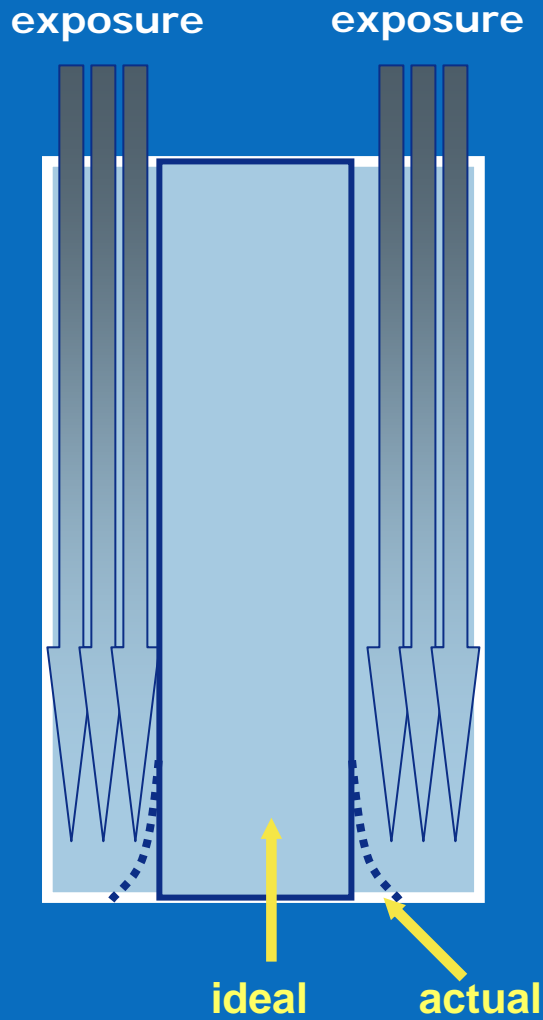
2nm resist molecules

Tomorrow's
2D problem

Source: Intel



Lithography at Nanoscale



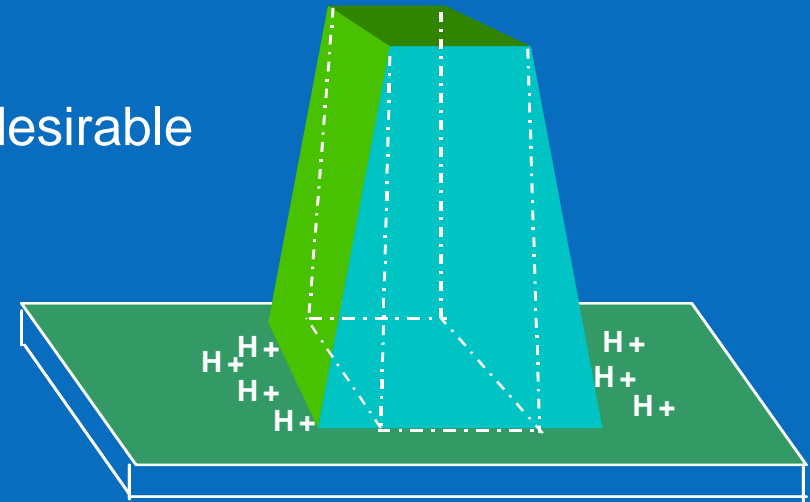
Tomorrow's 1D problem

- Resist thickness \gg feature size
- Absorption through resist changes effective dose and exposed profile
- Function of dose, contrast, diffusion, ...
- Accentuated as scale shrinks

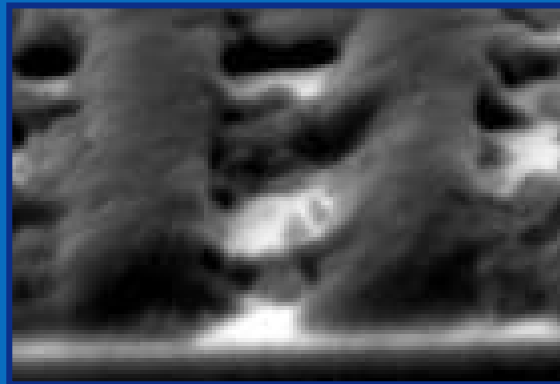
Designing Material Solutions

Solutions

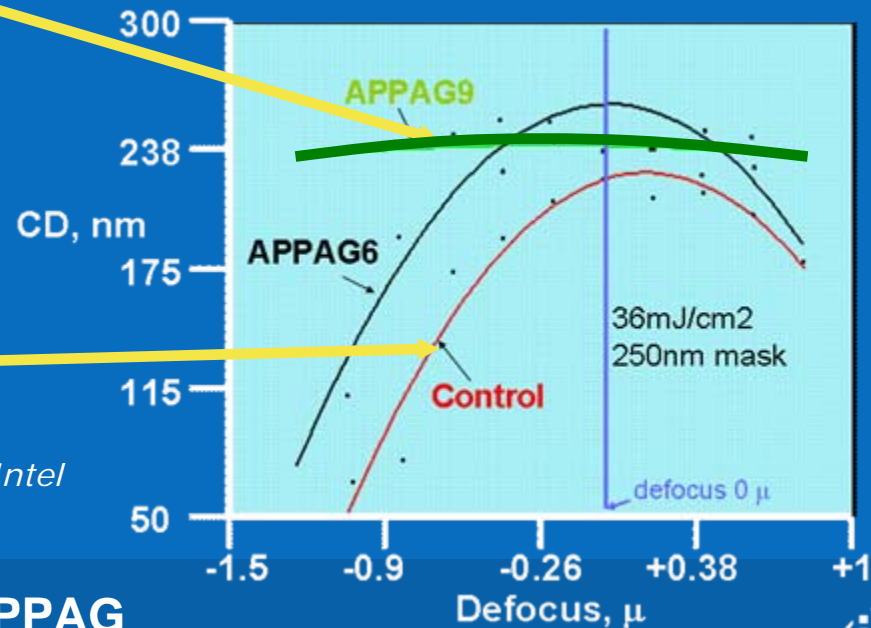
- Increase intensity or thin resist – not desirable
- **Modify surface to improve sensitivity**



Source: Intel



Source: Intel

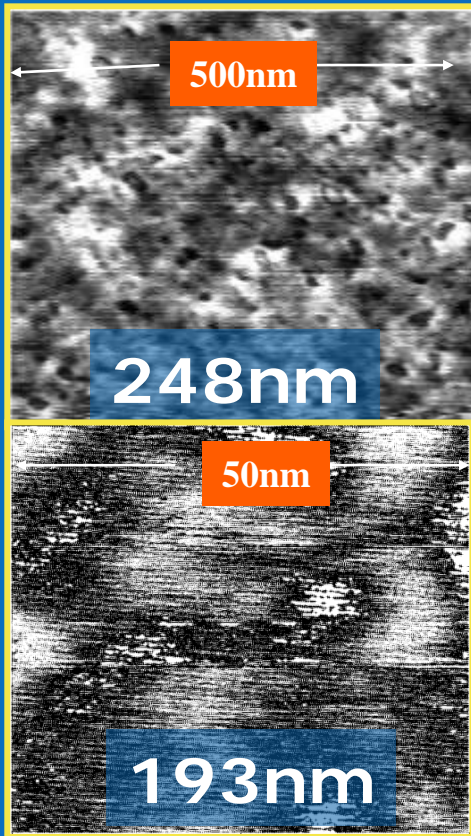


DUV @ 0.8 μ defocus
Experiment replaces BARC with APPAG

11/13/2006

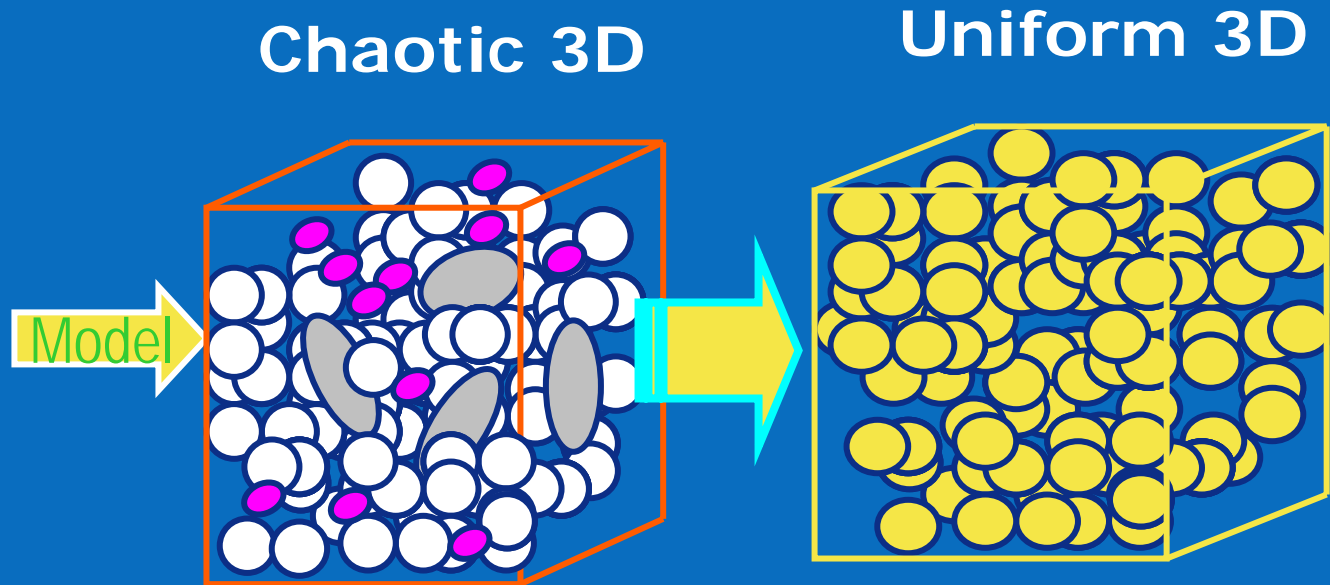


Resist pixel evolution



*chaotic anisotropy
by AFM*

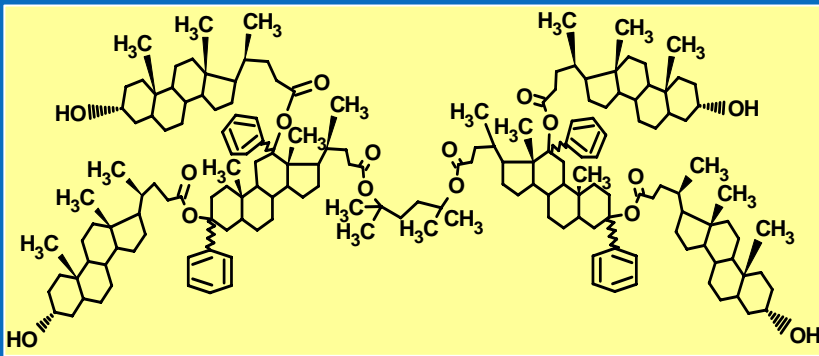
Source: Intel



Designing Material Solutions

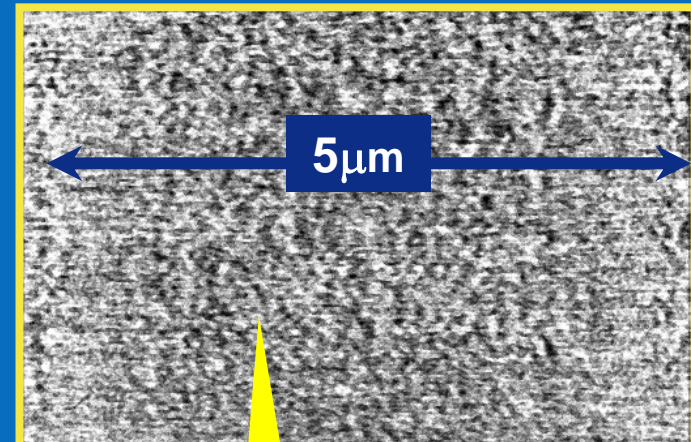
Resist solutions

- Improvement in uniformity
- Molecular size
- Self-assembly
- Designing active molecules



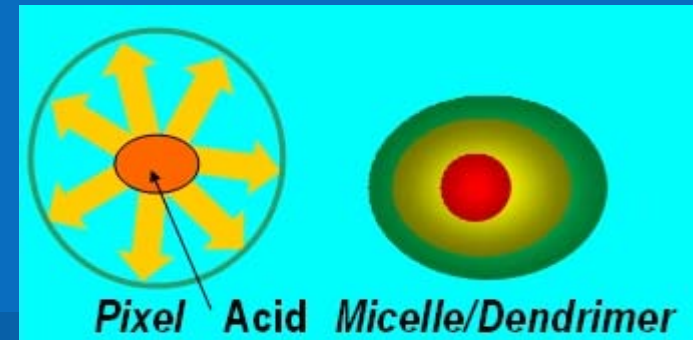
“G1” Dendrimer

These are small (1 to 2 nm) tree-shaped molecules that modulate host-guest chemistry by using different steroids and terminal functionality. When exposed, the dendrimeric host-guest system is ripped apart. This disruption in structure encourages the fragments to dissolve. Thus, it is an architectural approach to a preorganized nanometer sized lithographic pixel using a branched design



Dark regions detected by CFM are probably catalyst precursor or “PAG”, (photoacid generator) {AFM shows smooth surface}

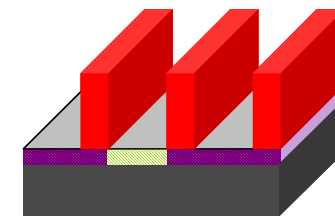
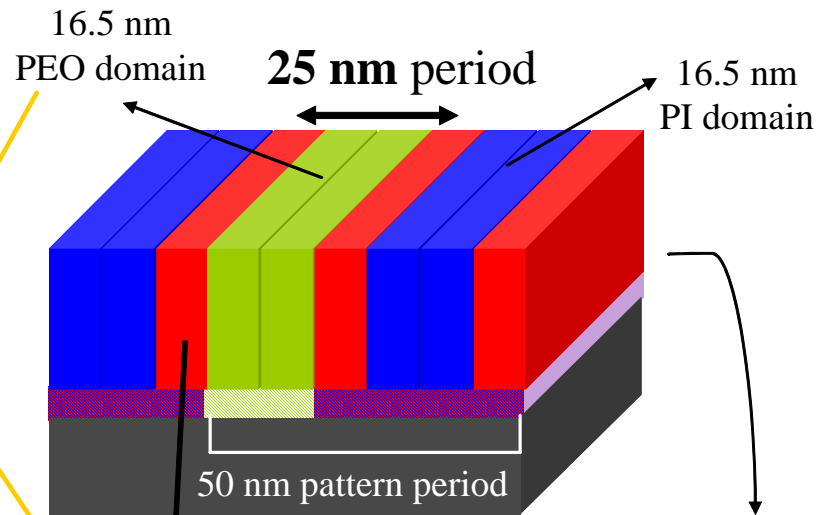
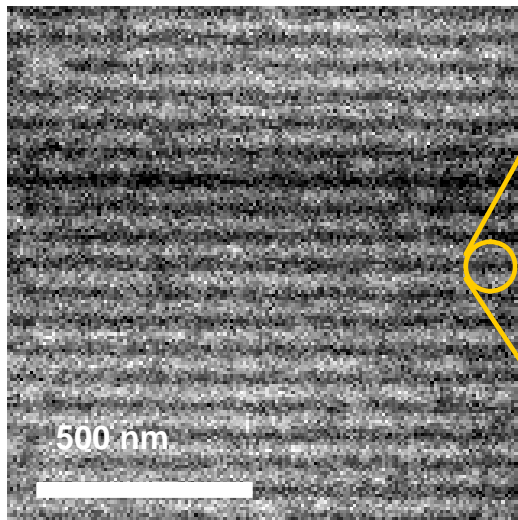
Source: NIST



Pattern Assisted Self-Assembly

Perfectly assembled triblock copolymer (PISO) on binary surface pattern

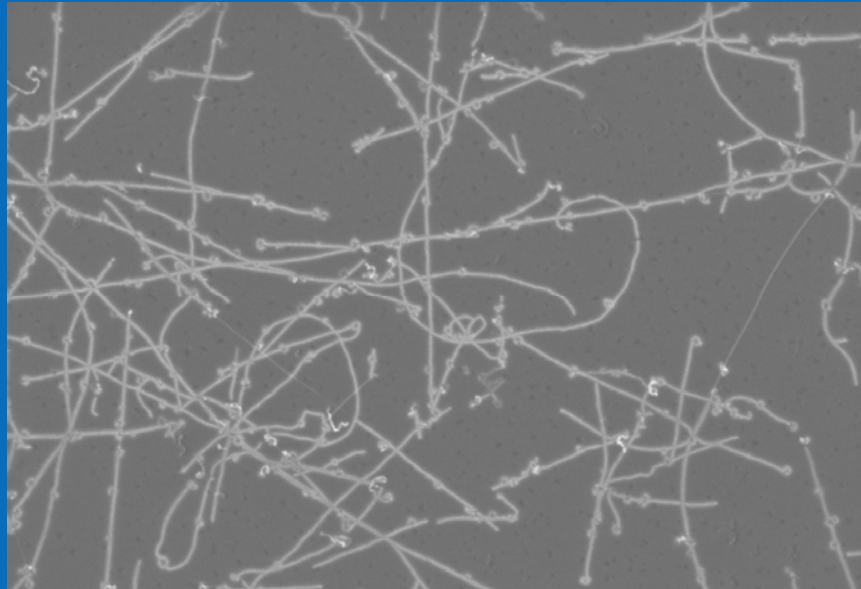
Assembled PISO



The possibility: Pattern at 50 nm; manufacture 8 nm features with a 25 nm period!

Welander, Chatterjee, Bates, de Pablo, Nealey

Daunting



Source: Intel

Possible

University of Wisconsin-Madison
NSEC
Nanoscale Science & Engineering Center

SRC

Directed self-assembly with block copolymer materials can fabricate nearly the entire basis set of essential features required for integrated circuits

Isolated Line ✓
Periodic Lines ✓
Bends ✓
Jog ✓
T-junctions ✓
Isolated Spots ✓
Periodic Spots ✓

Stoykovich, Kang, Park, Muller, de Pablo, Nealey

Source: Nealey et al, University of Wisconsin
Funding: SRC, NSF

Less buzz here

Need more here

Summary: Moving to Manufacturing

- Nanomaterials which can be formed in place are inherently easier to integrate and have fewer side concerns
 - 1D and 2D nano grown in situ are already used in production
- Applications which ease alignment requirements can more readily incorporate nanomaterials where advantageous
 - Example: spin on coatings incorporating 3D nano
 - Example: ordered arrays created by directed self-assembly
- Far more research work is needed to utilize 2D and 3D nanomaterials which are not formed in situ
 - Purification of starting materials and prevention of contamination
 - Environmental, health, and safety evaluations
 - Alignment of billions of individual elements – a daunting task

Closing Thought

Thomas Edison:

Opportunity is missed by most people because it is dressed in overalls and looks like work.